EMC
The art of compatibility
MICROCHIP
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Introduction

Rodger Richey
Senior Applications Manager

Thanks to all for the great feedback we received on our first issue. If you didn't receive a copy, you can download one from the Microchip Web site at:

http://www.microchip.com/stellent/groups/sitecomm_sg/documents/devicedoc/en021615.pdf.

In the first issue, we covered the basics of EMC including ESD, EFT and Latch-up. This issue of the EMC Newsletter focuses primarily on Printed Circuit Board (PCB) layout and related issues.

As the articles show, you can significantly affect the EMC performance of a system through layout. This not only includes the traces and vias connecting parts, but also the placement of parts on the board and the type and layout of ground planes and traces.

In the next issue, we will cover Electrical Fast Transients, or EFT. EFT is the primary source of problems in applications that use transformerless power supplies, since either line or neutral is directly connected to VDD or VSS of the microcontroller.

As always, your feedback is important. Please send any comments, requests for support, or ideas for future topics to: EMC@microchip.com.

In This Issue

These articles discuss the various circuits used in protection devices, transformerless power supplies, and layout and component placement to supress EFT.

Recommended Reading

EMC and the Printed Circuit Board: Design, Theory and Layout Made Simple
by Mark I. Montrose, ISBN 0-7803-4703-X

A good practical summary of all that can be done at the PCB level to achieve EMC compliance. Shows how and why RF energy is created and propagated on a PCB. The book describes the fundamentals of EMC theory and signal integrity and ways to handle these events.

The Importance of Capacitance

Rodger Richey
Senior Applications Manager

You will see that capacitors are mentioned in most of the articles of this newsletter. Capacitors are used to filter out noise on supply lines before it enters a device. The capacitor provides a low impedance path for shunting or diverting noise currents to ground. In this case, the placement and routing of the supply traces, capacitor, and device are crucial. As shown later, it is best to route the supply lines to the capacitor, then to the device.

When selecting capacitors as noise filters, you must always consider two important characteristics of the capacitor: maximum frequency limitation and self-resonance.

The maximum frequency limitation of various types of capacitors is shown in Table 1.

Self-resonance is the frequency at which a capacitor no longer behaves like a capacitor and instead becomes more like an inductor. Ensure that the type of capacitor you are using to filter out noise has a higher self-resonance frequency than that of the noise you are trying to filter out. Table 2 shows the typical self-resonance frequencies of various values of capacitance.

(continued on page 2)

Tips and Tricks

Know your components. The ideal behavior of resistors, capacitors and inductors is based on the frequency of the signals passing through them. The diagrams below show the ideal schematic, the actual schematic and the impedance/frequency response of each.

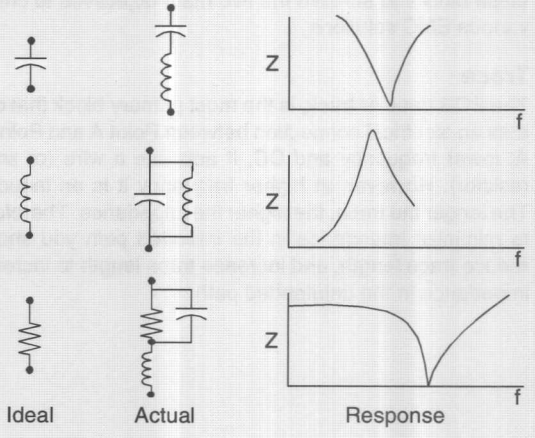


TABLE 1: CAPACITOR FREQUENCY LIMITS

Capacitor Type	Frequency Limitation
Aluminum Electrolytic	100 kHz
Ceramic	1 GHz
Mica	500 MHz
Mylar	10 MHz
Paper	5 MHz
Polystyrene	500 MHz
Tantalum Electrolytic	1 MHz

TABLE 2: SELF-RESONANCE FREQUENCIES

Capacitor Value	Leaded	Surface Mount
1 µF	2.5 MHz	5 MHz
0.1 µF	8 MHz	16 MHz
0.01 µF	25 MHz	50 MHz
1000 pF	80 MHz	160 MHz
100 pF	250 MHz	500 MHz
10 pF	800 MHz	1.6 GHz

Digital circuits are rich in noise. Fast edge rates and signals with periodic waveforms such as clocks tend to create noise. The primary reason is that the high frequency, fast edge rate signals induce high frequency current pulses on the voltage source. CMOS circuits are the worst because the N- and P-channel transistors used on the output pins are both on simultaneously (referred to as shoot-through) for a very short period of time when the pin changes state.

A decoupling capacitor will serve as a local "battery" for the device it is attached to. Oftentimes, on devices with multiple pins, decoupling capacitors will not be populated on all V_{DD} pins of the device. Frequently, these V_{DD} pins are not connected together inside the device; thus, the V_{DD} pins without the capacitors will not benefit from capacitors on other pins.

When used properly, capacitors can provide decoupling of unwanted signals and local power storage for circuits. Some might say that the capacitor is the worst enemy of EMC.

PCB Layout Fundamentals

Gaurang Kavaiya

Microcontroller Systems Group Manager

When talking about PCB layout, the first basic question that comes to mind is: "What is the primary goal?" The simple answer is: "Connect nodes."

Providing an electrical connection has been a primary goal of PCB layout since the invention of the PCB. However, when we talk about EMC performance, we need to add two more objectives.

- Minimize impedance in the intended path
- Maximize impedance in the unintended path

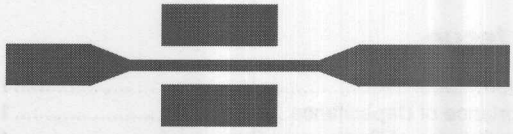
These objectives look simple; however, they define the heart of most EMC improvement tips. They use some basic PCB building blocks in the manner described above to achieve the intended results. Therefore, let's look at some basic building blocks of PCB layout. You can use these blocks to achieve the two main objectives to create various EMC solutions.

Trace

The PCB trace or track, is the most primary block that creates an electrical connection between Point A and Point B. At lower frequency and DC, it acts like a wire (or small resistor). However, at higher frequency it is an inductor. The longer the trace, the higher the impedance. Therefore, to minimize impedance in the intended path you should reduce trace length, and increase trace length to increase impedance in the unintended path.

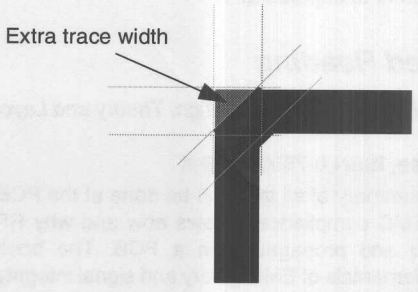
Trace Width

A wider trace width results in less impedance. It is obvious that the variation in trace width will cause impedance mismatch. Therefore, the trace width variation on the intended path can be harmful, but a similar variation in the unintended path can be beneficial.



Trace Corners

The 90-degree corner has the same effect as trace width variation due to the increased trace width at the corner (see figure below). Therefore, the same description applies here. The sharp angle also results in a field on the inner edge and may result in a higher amount of radiation.



(continued on page 3)

Vias

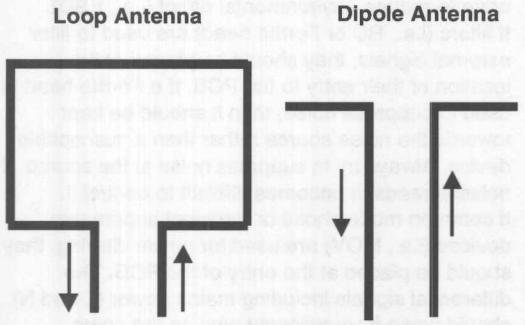
Each via introduces approximately 2 nH of inductance and 0.5 pF capacitance. Therefore, the introduction of multiple vias can have an adverse effect on the intended path, but they can be helpful in the unintended path.

PCB Capacitor

If you separate two conductors by dielectric, it creates a capacitor. In the case of a PCB, a conducting trace is separated by dielectric PCB material. This forms the capacitor. This parallel conductor can be on the same layer or a different layer. This capacitor value depends on geometry, dielectric material and separation. If this capacitor acts as a noise bypass (shunting) source, then it's helpful. However, if it acts as a coupling source, then it is harmful.

Antennas

When you create a PCB layout, you may create many hidden antennas. This is further discussed in the article **"Every Loop is an Antenna, Like It or Not"** on page 6. They exist in your layout but you may never realize it. For example, two of them are:



The radiation depends on frequency, current, area and inductance. These antennas can radiate, as well as pick up the high-frequency signal and can create some issues.

Transmission lines

By definition, a transmission line is a signal-carrying circuit with controlled electrical characteristics used to transmit high-frequency or narrow-pulse signals. On PCBs, it is a term referring to designing track layout to have accurately defined track impedance.

Transmission lines can easily be made on PCBs by controlling materials and dimensions and providing accurate termination resistances at source and/or load. They may also be extended off the PCB (if necessary) with appropriate controlled-impedance cables and connectors.

Two specific instances of a transmission line are:

- **Microstrip**

  A signal on a PCB, usually carrying high frequencies or with a very fast rise time, that is carefully dimensioned and laid over a ground return trace on an adjacent or both adjacent layers, to provide precise control of signal delay, track impedance, and end reflections.

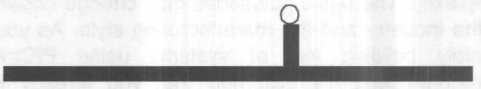
- **Stripline**

  A technique to tightly control the transmission line characteristics of a PCB trace by running parallel tracks for the signal and return path or differential pair.

The article, **"PCB Design Techniques for High-speed Digital Systems"** on page 8, provides more insight into this. You can also find lots of formulas and simulation models on this subject on the Internet.

Stubs

A stub is a short trace (see figure below) that is connected to a main trace.



If a stub trace exists without a terminating point, then it is an antenna, and its uncontrolled impedance may cause signal reflections with unpredictable and detrimental results.

In summary, we have discussed some basic building blocks of PCB layout. Each can be used in a positive or negative way. Many creative solutions can be created by using these building blocks to meet the two fundamental objectives explained earlier.

Let's look at one such example. If power traces (V_{DD} and GND) are run in parallel, then the created PCB capacitor is a really good quality continuous decoupling capacitor. The same concept applies in using two adjacent layers for the power and ground planes. However, the same PCB capacitor can have an adverse effect if you run two traces in parallel and one is carrying a sensitive analog signal while another is carrying a high-frequency clock.

When designing a board, I recommend the following procedure to achieve better EMC performance.

- Identify the power/ground sources and critical signals
- Partition the layout into functional blocks
- Position all components with critical signals adjacent to each other
- Route power and ground traces
- Route critical signals and their return paths
- Route the remainder of the board

I wish you "Happy Routing".

The Art or Science of Component Placement

Gaurang Kavaiya
Microcontroller Systems Group Manager

If you are looking to improve the EMC performance of your design, then PCB layout gives you the biggest "bang" for your "buck".

The first step towards achieving good layout starts with component placement. You cannot have a "good" PCB layout with "bad" component placement.

When talking about PCB layout, you might hear the acronym, DF_. Basically, the first two letters stand for "Designed For" and the third character (underscore) explains the determining factor. You may also hear the acronyms DFM (Designed For Manufacturability) or DFA (Designed For Assembly) and DFT (Designed For Testability). DFA focuses on reducing assembly error, while DFT focuses on providing adequate test coverage while minimizing the number of required test (probe) points, and placing test points to minimize test fixture complexity. The basic guidelines may change depending on the industry and the manufacturing style. As you are possibly building lots of systems using PICmicro® microcontrollers, it's assumed that you already know about these. If you don't, your manufacturing people will let you know ☺.

In this article we'll focus on another aspect – designing for EMC. When we talk about EMC some people call it an "art", while some people call it a "science". This article will look into some aspects of component placement art (or science).

The following suggested rules can be used when placing components:

- Start by drawing the PCB outlines and place all the components outside the PCB space.
- The next step in component placement is to identify the functionality and signals associated with the component.

  First, separate the components based on the associated functionality. For example:

  - Analog versus Digital
  - Supply versus Signal
  - Power Driver versus Signal Conditioning

  Then, separate them based on frequency and the power associated with it. For example, low frequency versus high frequency. You may need to use more granularity in complex systems. Also, identify critical signals in the system (i.e., Interrupt, Clock, etc.).
- Place the storage capacitor close to the location where demand is the highest. You should place multiple storage capacitors throughout the board. At a minimum, one per functional block and maybe more if instantaneous demand is high. A decoupling capacitor should be placed as close to the supply pins as possible. Use one decoupling capacitor per each power pin pair. The article, **"The Importance of Capacitance"** on page 1, provides more details on capacitor selection criteria.
- Place crystal oscillators and clocks next to the load (i.e., oscillator pin of microcontroller). Preferably use a guard ring around this block and connect it to Ground at multiple locations.
- Place the high-frequency source and destination components closer to make the high-frequency signal short. Similarly, try to minimize the trace length for critical signals (i.e., Interrupt, Reset, etc.).
- Preferably, high-frequency signals should be kept on the same board. If it is essential to send the high-frequency signal outside the board, then those components should be placed closer to an edge connector. Please use a transmission line to reduce reflection and radiation.
- The susceptible components should be kept away from the PCB edge. Preferably, place them in the center of the board. If this is not possible, try to place them at a distance greater than 25 mm from the edge.
- Components that interface with the external world should be kept close to the PCB edge. The remaining components should be kept away from PCB edge to reduce environmental effect (i.e., ESD).
- If filters (i.e., RC or Ferrite bead) are used to filter external signals, they should be placed at the location of their entry to the PCB. If a Ferrite bead is used to suppress noise, then it should be kept towards the noise source rather than a susceptible device. Always try to suppress noise at the source. If noise spreads, it becomes difficult to control it.
- If common mode choke or transient suppressor devices (i.e., MOV) are used for power filtering, they should be placed at the entry of the PCB. The differential signals including mains power (L and N) should come from adjacent pins on the same connector.
- Physically separate functional blocks to reduce coupling. Place noise generating devices and susceptible devices to the opposite end of the PCB, or try to have maximum distance between them.

In summary, we've discussed some basic rules for component placement. If you follow these rules, you have made the first step towards achieving a good PCB layout. You need to use these rules with your DFM rules and at some point, you may have to give one priority over the other. Figure 1 and Figure 3 on the following page illustrate this concept in graphical format.

FIGURE 1: FLOOR PLANNING SAMPLE 1

High Power / Frequency Components Placed Near Connector

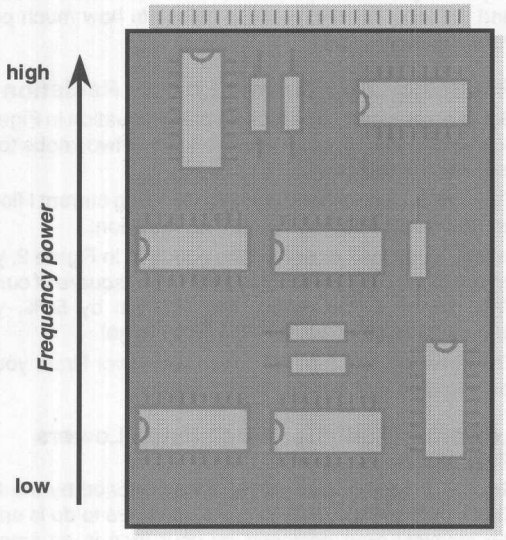


FIGURE 2: FLOOR PLANNING SAMPLE 2

Separate Digital and Analog Portions of the Circuit

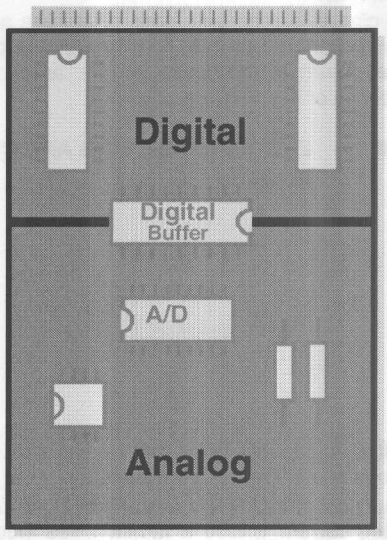
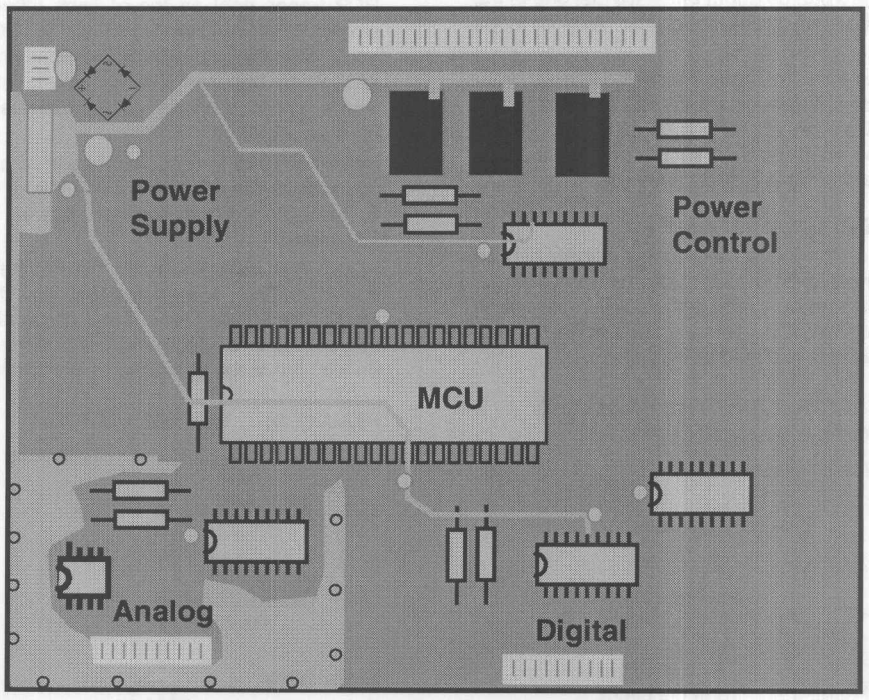


FIGURE 3: FLOOR PLANNING SAMPLE 3



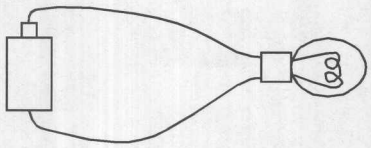
Every Loop is an Antenna, Like It or Not

Jan van Niekerk
Principal Engineer

Introduction

Electric circuits are current loops. Electrons are pushed out from the energy source, flow through the circuit, and ultimately return to the power source, as shown in the simple circuit of Figure 1.

FIGURE 1: ELECTRIC CIRCUITS ARE CURRENT LOOPS



Well, after that revelation, I have some bad news and some good news about current loops.

First, the bad news. Every current loop that carries an alternating current is also a radiator. Yes indeed, every circuit you have ever designed is a current loop, and therefore a loop antenna. Consequently, every circuit you have ever designed radiates radio frequency energy. There is nothing you can do about that – it's just one of the laws of physics. As a wise man once said; "All your loops are belong to us".

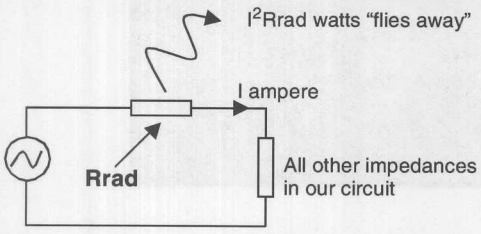
Now, for the good news. You have the choice to make your circuit a good loop antenna or a bad loop antenna. In an EMC situation, where radiation (or susceptibility) needs to be minimized, you want to make sure your loop is a bad antenna. So what makes a loop antenna "good" or "bad"?

Good Loop, Bad Loop

The "goodness" or "badness" of a loop antenna can be modeled by a single resistor. Let's call the model Rrad, which is short for "radiation resistance". Take a look at Figure 2. If we have an AC current of I ampere flowing, we can easily calculate the radiated power.

FIGURE 2: CALCULATING THE RADIATED POWER IN A CIRCUIT

Radiated Power = I^2 x Rrad



Now remember that this resistor is a model of radiated power. In a "normal" resistor, the I^2R power is transformed into heat in the resistor. In our model, Rrad does not actually get hot – it is a model for the radio frequency power that flies off into space – and makes you fail EMC testing.

So, there you have it. If you know the radiation resistance, and the loop current, you can calculate how much power your circuit radiates.

Reducing Loop Current Lowers Radiation

Being an engineer, and looking at the equation in Figure 2, you've already noticed there are at least two knobs to turn to lower the radiation.

The obvious knob to turn is the alternating current I flowing around the circuit – no current, no radiation.

In fact, if you look closely at the equation in Figure 2, you'll note that radiated power is related to the *square* of current. This means if you reduce loop current by 50%, you'll reduce radiated power by 75%. Way to go!

The other knob to turn is Rrad. If you lower Rrad, you will lower radiation. Let's see how it is done.

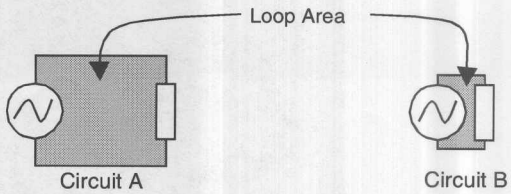
Lowering Radiation Resistance Lowers Radiation

Rrad is directly related to the *area* enclosed by the loop! That's all there is to it. Really! All you have to do is ensure the physical area enclosed by your loop is as small as possible. The area we are talking about is the open area surrounded by your sources, loads and interconnection wires or PCB traces. Oh, and by the way, if you put two PCB traces right on top of each other, the loop area is small, but still not zero – just turn the PCB on its edge and you'll notice a loop with one dimension being the vertical separation between the two layers of copper! In other words, you can never really make the loop area zero in practice – just very small.

Note that Rrad is a *cubic* function of area. This means if you reduce the area enclosed by your loop by a factor of 2, you reduce the radiated power by a factor of 8 (2 cubed).

Figure 3 shows the same circuit, composed of an AC current source, a load resistor, and the interconnecting wires. The shaded area is the physical area enclosed by the loop. Guess which circuit is better – and all you had to do was move the components a little closer to each other.

FIGURE 3: REVISED CIRCUIT



Summary

If you want to pass EMC testing, ensure current loops are small in area and/or carry small currents.

Further Reading

Microchip application note AN831, "*Matching Small Loop Antennas to rfPIC® Devices*", provides equations to calculate Rrad as a function of area, and some additional references.

Ground Planning Case Study

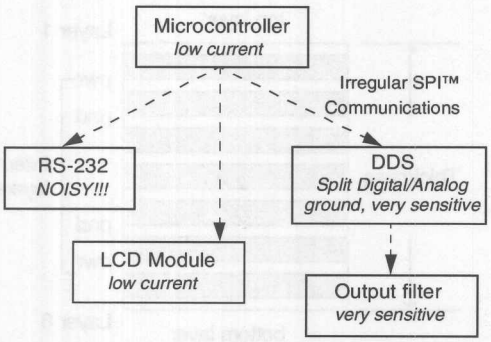
Joe Julicher
Principal Applications Engineer

Ground planning is a critical part of any non-trivial circuit board. A good ground layout will give resolution to analog converters, reduce EMI, improve EMI compliance, and insulate the designers from many nasty real world events. Like most skills, the ability to plan a good ground layout improves with practice, and therefore, should be applied for all designs.

A good ground plan starts with identifying the circuit elements. A design for a programmable frequency synthesizer would have the following components:

- A direct digital synthesizer (DDS),
- an output filter for the waveform,
- a microcontroller,
- an LCD module,
- and RS-232 communications.

Following is a block diagram:



In the block diagram, there are a few notes to help plan the ground.

The most critical device is the DDS and the output filter. Because the output filter is using a signal from the DDS, the ground path should be connected from the output filter directly to the DDS. This will ensure that any DDS noise is applied equally to the output ground and output signal. An external device using this signal generator will not see any noise because it will cancel.

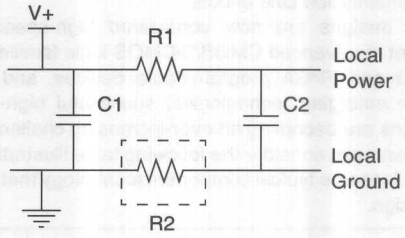
The RS-232 block contains a switched capacitor power supply to generate the RS-232 voltages. This is very noisy and involves relatively high currents so you must isolate this section carefully.

The ground plan will make use of three techniques for isolating noisy areas of the design:

1. Create an independent ground and power path to specific sections.
2. Bypass capacitors.
3. Isolation filters on power and ground.

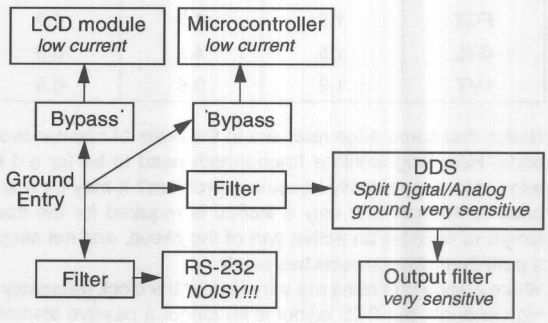
The first technique is fairly standard. It is represented in the ground plan by noticing where the ground path arrows start and end. This technique works by controlling the ground current paths, preventing sensitive sections from sharing a ground with noisy sections.

Adding bypass capacitors directly helps ground problems by providing a low impedance path for noise. Make sure that the bypass capacitors are chosen correctly for maximum effect. The microcontroller and the LCD module are fairly low current so their impact on ground will be low. Bypass capacitors are probably sufficient. Isolation filters are simple pie filters as shown below.



In many cases, R2 is not required so the ground path is not isolated. For some applications, R1 and R2 are replaced with RF chokes or inductors. The idea is to create a low impedance path for DC current but block unwanted noise. The DDS is very sensitive so it would be a good idea to use an isolation filter on the power and the ground for the DDS. This filter will produce a local ground that will be extended to the output filter.

Now that the isolation techniques are determined, the ground plan is produced. The plan below shows our first pass design. In this figure, the arrows indicate the power and ground paths.



After testing the board, it is now a simple matter to update our ground plan and make changes to the layout if there are any noise issues. This ground plan should be included in the schematics and the layout engineer should ensure that the plan is followed.

A successful ground layout will help speed your product to market. The key to good layouts is experience and documentation, so start today.

PCB Design Techniques for High-speed Digital Systems

Al Rodriguez
Principal Engineer

High-speed systems require the design of the PCB to be considered early in the design cycle. The PCB design must be planned and not left to chance. A design that is not planned may result in a system that is plagued with intermittent failures and degrades system operation as well as performance.
The design engineer must address the following:

- Power Distribution system,
- Signal Interconnections, and
- Transmission Line effects

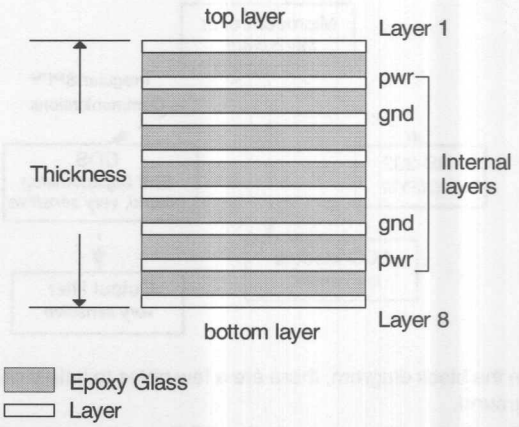
Most designs are now considered high-speed. With the advent of advanced CMOS/BiCMOS logic families, countless CPLD and FPGA programmable devices, and newer and faster emerging technologies, successful high-speed PCB designs are becoming an ever-increasing challenge.
For example, consider the following table illustrating the edge rates for some typical component technology that may exist in a design.

Family	Buffer Speed tprop (ns)		Rise/Fall (ns)
	min	max	
ABT	1.0	3.6	0.5
AC	1.5	8.5	3.0
ACT	1.5	7.5	3.5
AHC	1.0	10.0	2.5
AHCT	1.0	8.5	6.0
ALVC	1.0	6.0	0.3
CBT	—	.25	0.5
FACT	3.0	5.0	3.0
FCT	1.5	4.5	4.6
GTL	1.5	4.2	0.6
LVT	1.2	3.6	0.5

Notice that some edge rates are in the order of sub-nanoseconds. How long would a trace length need to be for a 1 ns edge rate to potentially become a problem? It may be a surprise to find out that only 3 inches is required for the trace length to become an active part of the circuit, and not simply a path that interconnects two points.
When pulse edge rates are very fast, or the clock frequency is high enough, the PCB layout is no longer a passive element. The fast slew rates contribute to noise generation in the form of signal reflections, crosstalk, and ground bounce.
The typical high-speed PCB consists of a glass laminate (0.062 mils thick) with epoxy resin, generally referred to as FR-4 material. It is bonded by a one-ounce copper foil for each layer and can be many layers for multi-layered boards.
A circuit trace has a characteristic impedance associated with it, and the impedance depends on the width and thickness of the trace, as well as the PCB dielectric constant (E_r) of the material used (FR-4), and the height between the trace and reference plane.

Figure 1 shows a cross-sectional view of a PCB and depicts a multi-layer board with Microstrip and Stripline transmission line layouts. Microstrip refers to the trace routed on the outside layers of the PCB. Stripline refers to the trace routed on the inside layers of a PCB, and is between two voltage reference planes.
An eight-layer board stack-up configuration with four layers used as planes improves EMC performance by utilizing the additional power and ground layers for isolation rather than for signal routing, and because of the additional ground plane, the ground impedance is reduced.
In this configuration, the signal layers are next to planes, and the layers are strongly coupled together. The high-speed signals should be buried between the planes providing shielding to reduce the emissions from these signals.

FIGURE 1: MULTI-LAYER PCB CROSS-SECTION



Power Distribution

The design engineer must address the transient current demands placed onto the power distribution system.
Low-impedance planes must be used to distribute power and reduce inductance. The usage of power planes additionally provides isolation from coupled noise.
The power plane impedance is important for PCBs with high-speed logic, and more care is required due to increased common impedance coupling. The instantaneous current generated with the rising and falling edge of a logic device output, causes the power plane to ring and is aggravated with higher switching speed and simultaneous outputs switching.
To reduce low frequency noise, filter and distribute power to all devices. Use a bulk capacitor (10-100 µF) near the source where power comes into the board, and place high frequency decoupling capacitors (0.1 µF) as close to the power pins of the device.
To reduce impedance, use device packages with lower pin inductance (TSSOP versus DIP), and limit the number of device drivers in a given package. Use of sockets or carriers should be avoided.

(continued on page 9)

Signal Interconnections

PC boards with multiple signal layers provide high signal density but increase the probability of coupled noise. For this reason, measures should be taken to reduce noise.

ROUTING SCHEMES

Signals should be grouped together into categories based on wave shape control requirements and crosstalk limits. For example, clock signals and strobes require the highest degree of isolation from crosstalk since they have wave shape control requirements.

Routing order is vital. Generally, clock signals should be routed with controlled impedance and must not branch or have long stubs. Avoid using vias, as they will cause impedance changes and generate reflection.

Clock signals must be isolated and confined between reference plane levels. Do not allow other signals to be routed in close proximity to clock lines and ensure that clock lines have extra spacing between adjacent lines.

Segregate critical signals (such as clock and strobes) into separate packages and use devices with slew rate control.

TRANSMISSION LINE EFFECTS

Signal reflections, crosstalk, and ground bounce are effects caused by improper management of high-speed signals at the PCB level.

SIGNAL REFLECTIONS

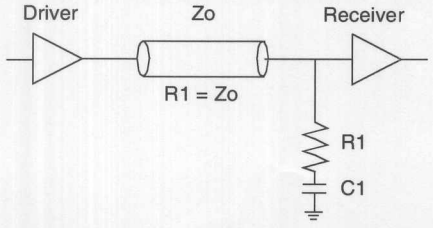
Signal reflection refers to a signal that propagates along a trace line and reflects from any part of the line that is different. The reflections combine by adding and subtracting from each other and cause the original signal or pulse to be distorted. These reflections occur from impedance mismatches and cause the receiver device to falsely interpret logic levels.

Proper signal termination minimizes signal reflections because the energy is absorbed completely. There are several signal termination schemes, each one appropriate to the type of application and each one offering different advantages. AC and Differential Trace Termination are two of the most general-purpose type of terminations.

AC Termination is preferred over other types of terminations (such as series or parallel). AC Termination has a capacitive load in series with the resistive load of the driver. Figure 2 depicts AC Trace Termination.

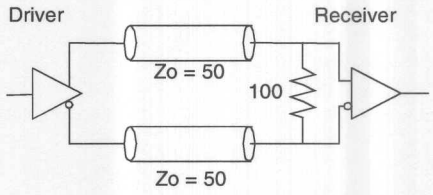
Series termination increases the rise and fall times and will control signal reflections, but may not yield the performance required.

FIGURE 1: AC TRACE TERMINATION



Differential Trace Termination requires a resistor between the signals at the receiving end of the device. The resistor should match the differential load impedance. Figure 3 depicts Differential Trace Termination.

FIGURE 2: DIFFERENTIAL TRACE TERMINATION



Route the two traces of a differential pair as close to each other after they leave the device. Also, maintain a constant distance between the two traces over the entire routing length.

CROSSTALK

Crosstalk is the unwanted coupling of signals between two traces running in parallel. A voltage change in one trace gets coupled to the adjacent trace by stray capacitance between them. Use extra wide spacing between adjacent signals to minimize coupling. If signals are susceptible to crosstalk, they should be run at right angles to one another.

GROUND BOUNCE

The load impedance, lead inductance, and the number of switching outputs are the factors that influence the magnitude of ground bounce in systems. Limit the number of drivers in a given package from driving heavily loaded signals. If several drivers in a package are used to drive critical signals, do not mix with other logic that switches outputs simultaneously. In most FPGAs, the outputs have slew rate and drive current control. Do not be tempted to use the fastest slew rate and the maximum drive current. Generally, manufacturers provide guidelines as to the maximum number of outputs that can switch simultaneously at a given current drive.

There are Electronic Design Automation (EDA) tools available to help the engineer explore a design and define layout rules with respect to signal integrity. These tools help identify areas that may need termination.

Taking appropriate measures and considering fundamental electrical principles, as well as using EDA tools to identify potential problems, will prevent system failures resulting from improper high-speed PCB layout.